Increasing reticle inspection efficiency and reducing wafer print-checks at 14nm using automated defect classification and simulation

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ABSTRACT

IC fabs inspect critical masks on a regular basis to ensure high wafer yields. These requalification inspections are costly for many reasons including the capital equipment, system maintenance, and labor costs. In addition, masks typically remain in the "requal" phase for extended, non-productive periods of time. The overall "requal" cycle time in which reticles remain non-productive is challenging to control. Shipping schedules can slip when wafer lots are put on hold until the master critical layer reticle is returned to production. Unfortunately, substituting backup critical layer reticles can significantly reduce an otherwise tightly controlled process window adversely affecting wafer yields.

One major requal cycle time component is the disposition process of mask inspections containing hundreds of defects. Not only is precious non-productive time extended by reviewing hundreds of potentially yield-limiting detections, each additional classification increases the risk of manual review techniques accidentally passing real yield limiting defects. Even assuming all defects of interest are flagged by operators, how can any person's judgment be confident regarding lithographic impact of such defects? The time reticles spend away from scanners combined with potential yield loss due to lithographic uncertainty presents significant cycle time loss and increased production costs

An automatic defect analysis system (ADAS), which has been in fab production for numerous years, has been improved to handle the new challenges of 14nm node automate reticle defect classification by simulating each defect's printability under the intended illumination conditions. In this study, we have created programmed defects on a production 14nm node critical-layer reticle. These defects have been analyzed with lithographic simulation software and compared to the results of both AIMS™ optical simulation and to actual wafer prints.

Keywords: ADC, simulation, inspection, photomask, reticle, defect, disposition, wafer, CD, requalification

1. INTRODUCTION

The use of Automated Defect Classification & Analysis systems to review reticle inspections have started to make their mark in the industry. While speed and accuracy are the main pillars of an ADC system, their use in managing and accessing reticle inspection information is becoming a powerful tool for engineering analysis. The ability to integrate a reticle's inspection information across different inspection tool platforms, allows the reticle engineers and the tool operators to perform their daily tasks with more ease, speed and confidence. As these systems mature in their reliability, the reticle engineers are becoming more familiar with their use and finding new ways to use these systems to improve reticle efficiency and quality. This paper focuses on the adaptability of AVI's ADAS system to create these opportunities in a HVM leading-edge semiconductor facility.

2. MOTIVATION

One of the motivations for this paper was to improve the reliance of ADAS classification of erroneous false defects, referred to as "White Spots (WS)". If high reliability can be achieved via the ADAS software to accurately classify these false detections, then it would be possible to reduce the post inspection image captures, which are currently used to help judge if a WS detection is real or false. Eliminating these post inspection image captures would effectively increase reticle tool throughput.

Secondly, the ADAS inspection data management was modified to fit SAS model of reticle management. This created an opportunity to roll-out new functionality to assess if new quality gains can be realized. One aspect of which was to create a database to check for incorrect recipes used for reticle inspections. Though this function was not intended to attack the root cause of selecting incorrect inspection recipes, its intent was to highlight and document the errors. The function was also designed to be more "operator friendly", where ADAS can help the operator identify the errors and provide the correct recipes that needs to be used by the operators.

The third objective was to evaluate the accuracy of the simulation function by verifying the ADAS simulation results to AIMS™ and Wafer Print tests, using a 14nm reticle where different size programmed defects were placed in dense L/S pattern areas.

3. BACKGROUND

Automatic Defect Analysis System (ADAS) is a PC-based software product that automatically analyzes results from reticle inspection tools and quickly classifies defects, separating false from real, allowing the operators to focus only on defects of concern.

ADAS also simulates how the defects will affect the wafer CD to help remove classification doubt. Figure 1 shows a sample data flow on how the server interfaces with other systems in the wafer fab. The server scans reticle inspection tools looking for new or updated inspections and downloads the inspection results. The inspections are analyzed in seconds and results are then available for operators to verify using in-fab review stations. Engineers and managers can also view or change results on any Windows-based computer at their desks.

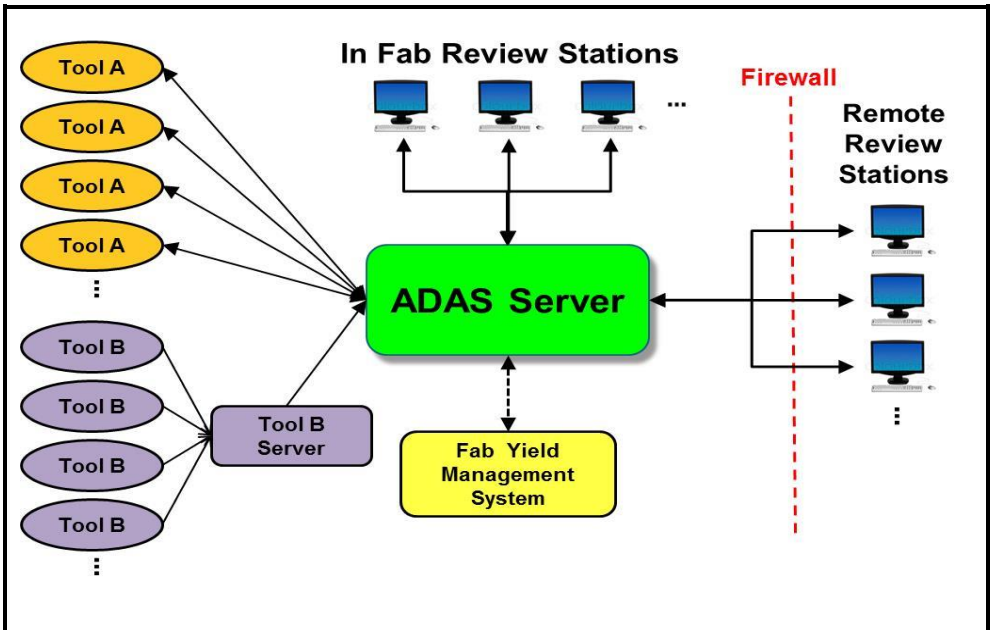

Figure 1 - ADAS data flow path

4. EXPERIMENT AND RESULTS

4.1 White Spot Detection Verification

One difficulty with inspection tools is the generation of random false detections, referred to as White Spots. All reticle inspection tools that use TDI sensors generate these false defects that are randomly generated in the sensors. While the inspection tool vendors continue attempting to reduce the occurrence of these detections, they still exist, and a post inspection defect image is taken to determine if they are real or false (see Figure 2). This is achieved by an operator keeping the reticle on the inspection tool to capture all the post-inspection images and re-classify the reticle inspection. This degrades reticle inspection throughput and reticle Turn-Around-Time(TAT) to the fab.

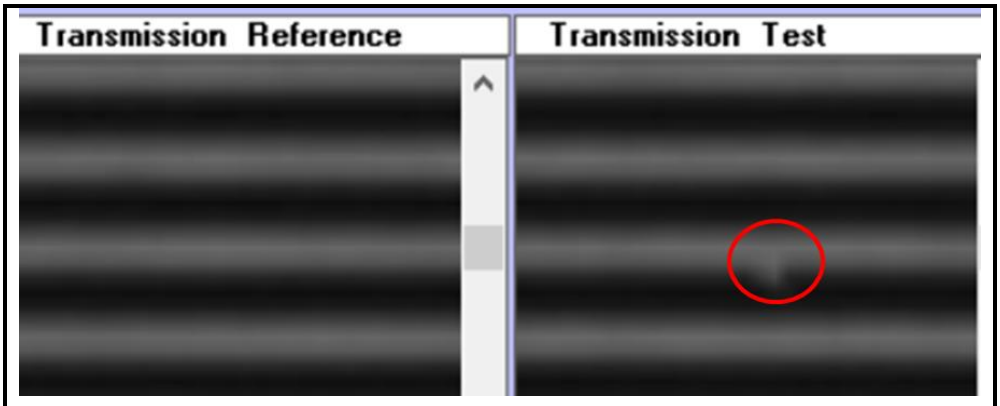

Figure 2 - White Spot False defect

The approach pursued was to create an ADAS software version that will be robust in accurately classifying White Spot detections, without the needs for post-inspection images. After several incremental improvements, AVI was able to achieve 96% accuracy, for matching to actual White Spots. Figure 3 shows the improvements over numerous software revisions.

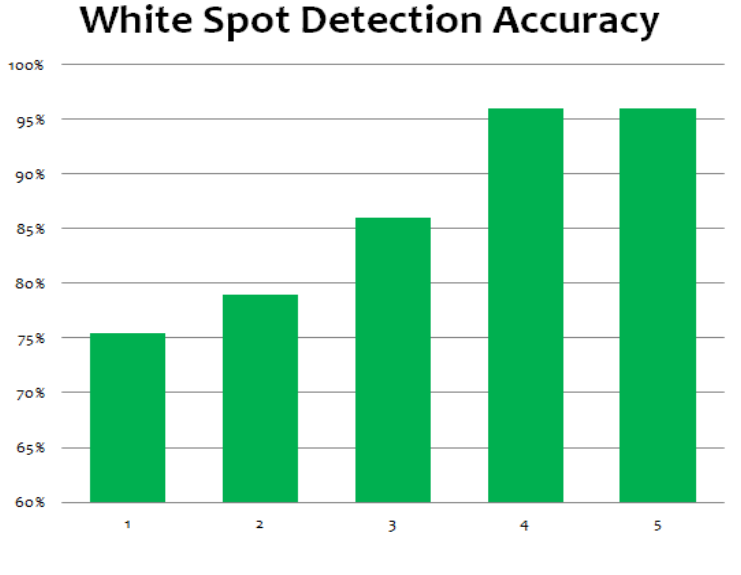

Figure 3 – White Spot detection improved over time

The introduction of the new ADAS s/w version was rolled out to production in August of 2014. The equipment mode for taking post-inspection images was turned off with procedures in place to allow occasional post-inspection image captures. The operators were trained to use ADAS as a way to verify if detection was real or was considered a White Spot. Figure 4 shows a substantial reduction in the time spent at the tool to capture post-inspection images. This resulted in a 97% reduction in post-image capture time in August, which translated into a 10% improvement in inspection capacity (see Figure 4.)

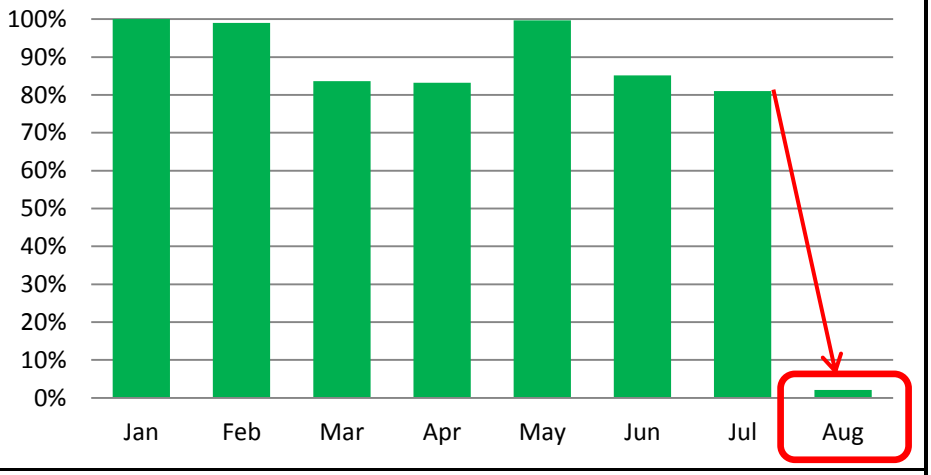

Figure 4 - Avg. time spent per reticle for post inspection image captures

4.2 ADAS Recipe Check

ADAS offers a robust inspection data management tool called the "File List." Every inspection run is stored in this location. Building on this platform, new features have been created including one that highlights any incorrect recipes used by an operator. Since the File List is updated every few seconds, operators are able to visually see the use of an incorrect recipe. The visual message is created under the Status column in the File List (see Figure 5a). In addition, the error is recorded permanently in the inspection report generated by ADAS as shown in Figure 5b. This was a critical, short-term solution, enabling Samsung to ensure the quality of reticle inspections.

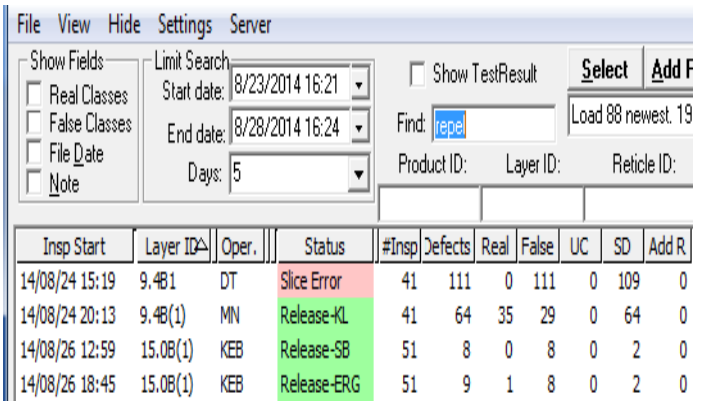

Figure 5a Status column shows "Slice Error"

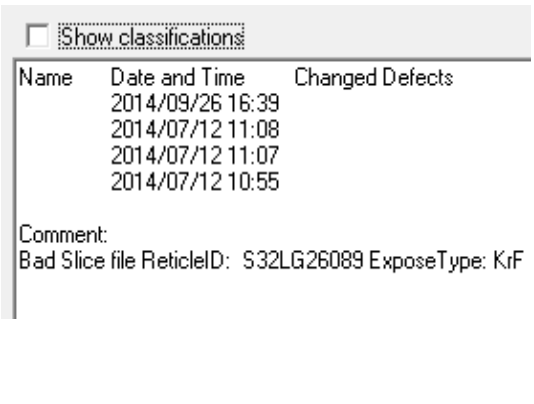

Figure 5b Event is logged in the inspection report

The most interesting outcome after the launch of this feature was its positive impact in operator performance. The recipe check served as a friendly, non-judgmental, and objective way of informing the operators if errors had been made. This resulted in over a 50% reduction in the errors being made for recipe selection (see Figure 6) which directly improved Reticle TAT and equipment efficiency.

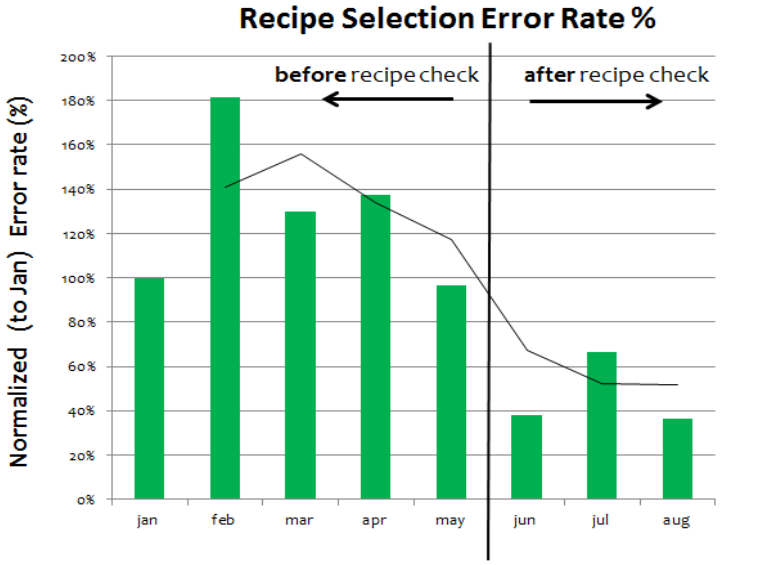

Figure 6 – Recipe selection error rate normalized to January

4.3 14nm Simulation

In order to test ADAS simulation, a 14nm metal layer production mask was modified by adding programmed defects using an advanced SEM repair tool. The defects were all placed near edges of a dense line space pattern on the mask and ranged in size from 40x40nm to 80x160nm (See Table 1)

Defect Width nm	Defect Length nm	Defect Width nm	Defect Length nm
40	40	50	50
40	40	60	60
45	45	80	80
50	50	40	80
60	60	45	90
80	80	50	100
45	45	60	120
40	80	80	160
45	90	60	50
50	100	80	160
60	120	60	60

Table 1 – List of programmed defect sizes

Figure 7a shows a SEM image of one of the programmed defects on the mask while Figure 7b shows an SEM image of the wafer after develop.

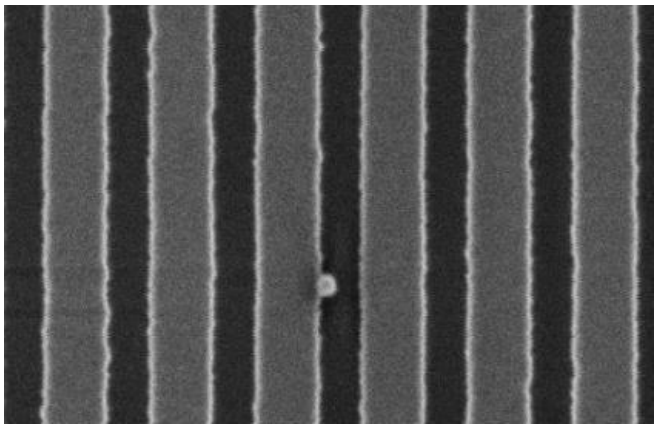

Figure 7a – SEM image of programmed defect on mask

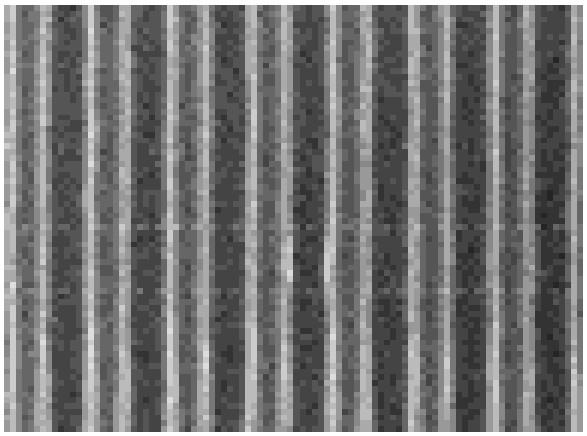

Figure 7b – SEM image of wafer after develop

Figure 8a shows ADAS defect simulation prediction with Figure 8b showing AIMS simulation prediction.

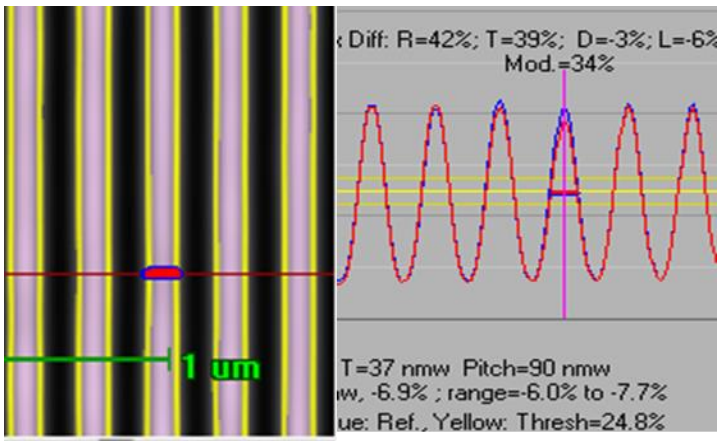

Figure 8a – ADAS Simulation Prediction

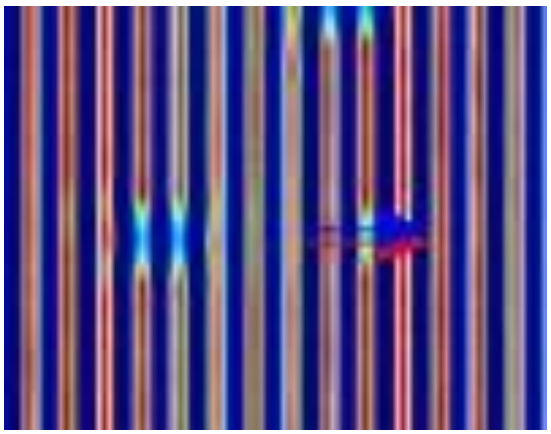

Figure 8b – AIMS Simulation Prediction

The results of the wafer after develop measurements, AIMS, and ADAS simulation results are all shown in Table 2. Applying a pass/fail threshold of 5% CD error is shown in the right three columns. Note that all three percentage CD error measurements result in the same pass/fail results except for defect number 21. ADAS is underestimating the CD percentage error of this defect.

	AIMS	ADI	ADAS	AIMS	ADI	ADAS
1	1.0%	5%	-0.5%	pass	pass	pass
2	0.0%	-2%	2.6%	pass	pass	pass
3	-2.8%	2%	-2.6%	pass	pass	pass
4	-3.4%	-4%	-3.0%	pass	pass	pass
5	-30.6%	-31%	-23.8%	fail	fail	fail
6	-39.0%	bridge	-34.5%	fail	fail	fail
7	0.0%	3%	-2.0%	pass	pass	pass
8	-2.5%	0%	-2.5%	pass	pass	pass
9	-25.1%	-17%	-21.3%	fail	fail	fail
10	-24.7%	-16%	-22.6%	fail	fail	fail
11	-61.4%	bridge	-63.0%	fail	fail	fail
12	bridge	bridge	bridge	fail	fail	fail
13	0.0%	-2%	-3.6%	pass	pass	pass
14	0.3%	5%	-0.6%	pass	pass	pass
15	-2.3%	-2%	-2.9%	pass	pass	pass
16	-8.2%	-5%	-6.9%	fail	fail	fail
17	-20.2%	-14%	-12.1%	fail	fail	fail
18	-38.1%	-31%	-23.0%	fail	fail	fail
19	-0.3%	1%	-2.4%	pass	pass	pass
20	0.3%	1%	-2.1%	pass	pass	pass
21	-7.9%	-7%	-4.9%	fail	fail	pass
22	-15.6%	-14%	-10.6%	fail	fail	fail
23	-47.1%	bridge	-36.2%	fail	fail	fail
24	bridge	bridge	bridge	fail	fail	fail

Table 2 – Percentage CD error from AIMS, Wafer, and ADAS

Figure 9 shows the percentage CD error prediction of ADAS vs AIMS from all programmed defects. Notice that in general, ADAS is under-predicting the error of most defects. This is atypical behavior for ADAS. Past data[1] has shown that ADAS typically matches or slightly over-predicts as compared to AIMS. This new under-prediction is unacceptable behavior, and demanded further investigation.

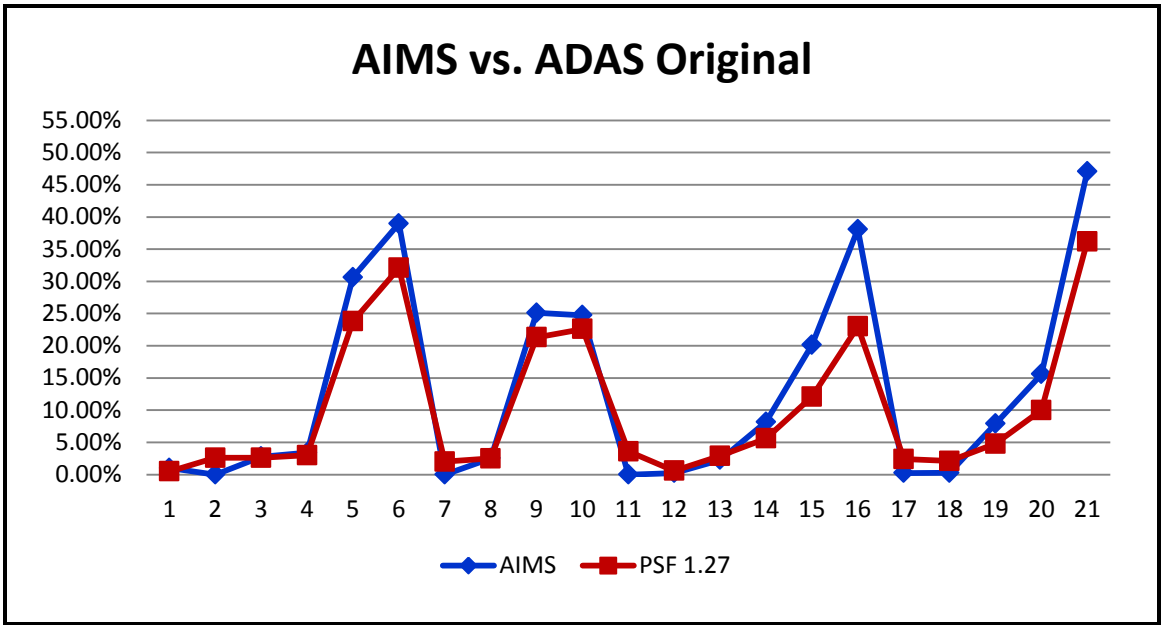

Figure 9 – Initial results show that ADAS is underestimating the percentage CD error compared to AIMS

Close analysis of all data identified an anomaly. The peak-to-peak intensity modulation predicted by ADAS was approximately 13% lower than that of AIMS as shown in Figures 10a and 10b.

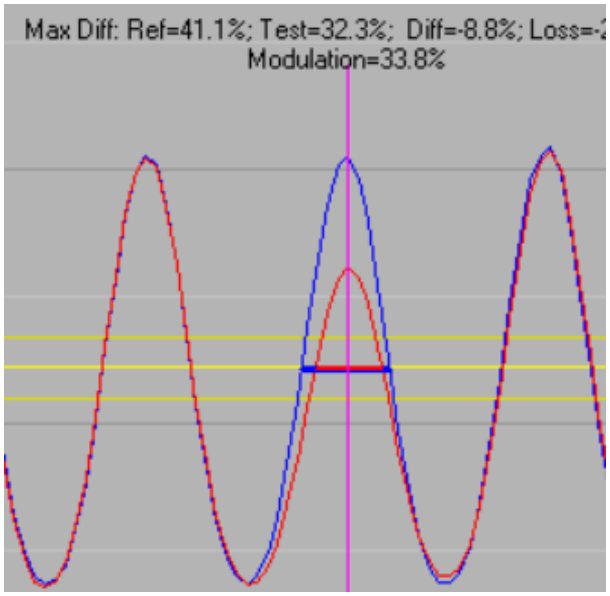

Figure 10a – ADAS modulation 33.8%

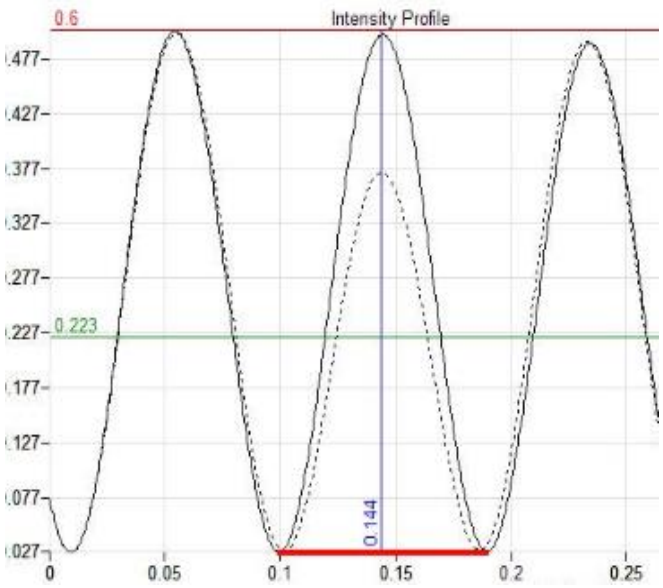

Figure 10b – AIMS modulation 47%

AVI engineering determined that the ADAS polarization compensation had not been optimized for 14nm node features. This parameter was adjusted until ADAS intensity modulation was equal to that of the AIMS modulation. The percentage CD error was then reanalyzed by ADAS with the results shown in Figure 11.

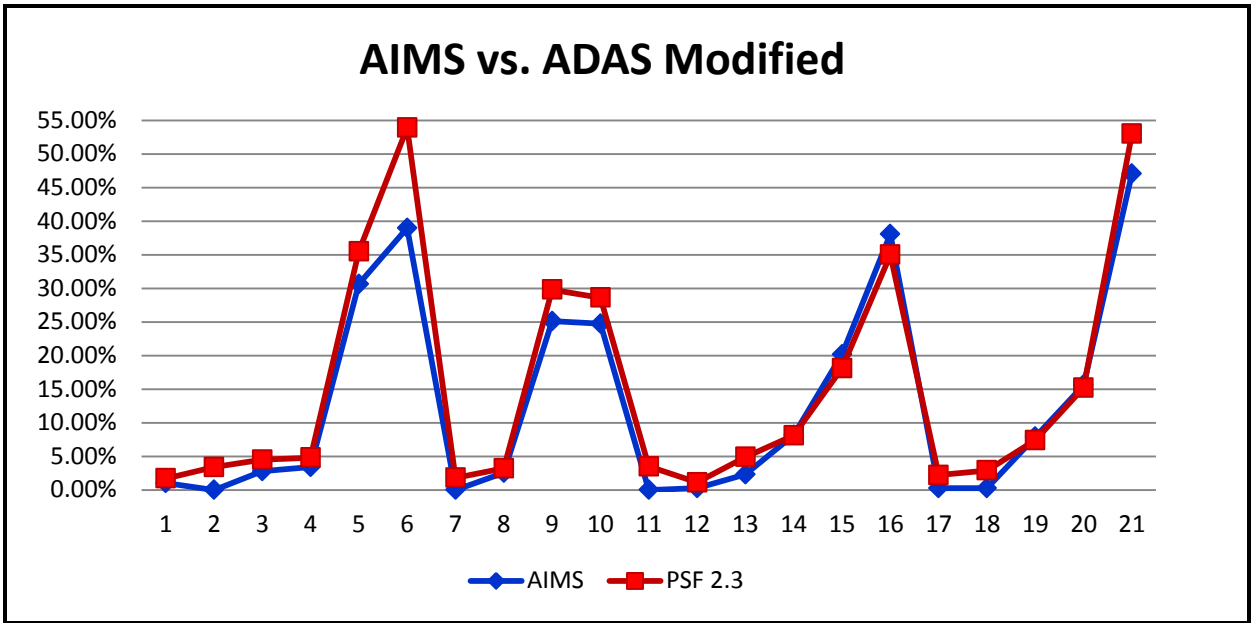

Figure 11 –ADAS results after modifying polarization compensation

The results showed that ADAS was once again matching or slightly over-predicting errors as compared to AIMS results.

5. SUMMARY AND CONCLUSIONS

Inspection tool recipe confirmation along with a 10% improvement in throughput, were both achieved in less than 6 months from concept to production release. During this same time frame, 14nm node defect simulation was tested using a production mask modified with programmed defects, measured with AIMS, and printed to wafer. Initial data showed an unacceptable amount of under prediction by ADAS percentage CD error. Modifying the polarization compensation factor increased modulation and brought ADAS back to matching or slightly over predicting percentage CD error. The result is more accurate inspections, increased tool throughput, and confirmation that ADAS simulation is ready for 14nm production.

6. FUTURE WORK

The authors plan to continue testing/improving ADAS simulation on 10nm node process once test masks are available and fine tune simulation models for all critical 14nm node wafer levels.

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